

REMARKS

Claims 1-38 are pending and rejected by the examiner. Claims 1, 8 and 32 are independent claims.

Applicants amended the abstract of the invention. The amended abstract does not exceed 150 words in length and clearly enables the United States Patent and Trademark Office and the public generally to determine quickly from a cursory inspection the nature and gist of the technical disclosure. No new matter was added.

The examiner rejected claims 1-38 under 35 U.S.C. §112, second paragraph, as being indefinite.

Claims 1, 8 and 32 recite "an out-of-order microinstruction pointer (μ IP) stack." As described in applicants' specification as originally filed, "(t)he μ IP stack 100 is an out-of-order stack where values are placed on the stack and removed from the stack before it is known if the sequence of operations were valid." (page 5, lines 17-20) Microcode executes in the micro core and performs microoperations, while microinstructions are used to manipulate the microinstruction pointer stack.

Applicants have amended the claims to clearly point out and distinctly claim applicants' invention. No new matter was added.

The examiner uses Kainaga to reject claims 1, 8 and 32 as having been anticipated.

Claims 1, 8, and 32 recite "an out-of-order microinstruction pointer (μ IP) stack," or similar language. Kainaga neither describes nor suggests at least this quoted claim feature.

Kainaga discloses a numeral 50 denotes a stack unit 50, a stack area 52, a stack pointer 51 for pointing to a storage address when a new storage request is issued to the stack area, and a stack pointer modifier 54. (col. 2, lines 57-62) These are very different from applicants' out-of-order microinstruction pointer (μ IP) stack. As described in applicants' specification:

The out of order execution core 18 includes an out of order microinstruction pointer (IP) stack 100. In general, a stack is a data area or buffer used for storing requests that need to be handled. A stack is typically a push-down list, meaning that as new requests come into the stack, the stack pushes down older requests. Another way of looking at a push-down list - or stack - is that a program usually takes its next item to handle from the top of the stack, unlike other arrangements such as "FIFO" or "first-in first-out" buffers. The stack 100 is implemented in a microcode environment. This allows fast subroutine returns in microcode. It also allows fast assist returns in microcode. (page 5, lines 3-13)

The μ IP stack 100 is different from a macroinstruction stack in several ways. For example, the μ IP stack 100 is not visible from a system level (i.e., the μ IP stack 100 cannot be directly manipulated from macrocode). The μ IP stack 100 is an out-of-order stack where values are placed on the stack and removed from the stack before it is known if the sequence of operations were valid. Thus, a set of recovery mechanisms is required to correct a sequence of operations that are later determined to be incorrect. The process of manipulating the stack (PUSH, POP, etc.) is very different from a traditional macroinstruction stack because of the out-of-order nature of the stack 100. (page 5, lines 14-23 and page 6, lines 1-2).

Accordingly, claims 1, 8 and 32 are not anticipated by Kainaga.

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific rejection, issue or comment does not signify agreement with or concession of that rejection, issue or comment. In addition, because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this

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paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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